



Dual, 8-Bit, 40MHz, Current/Voltage, Simultaneous-Output DACs

MAX5186/MAX5189

General Description

The MAX5186 contains two 8-bit, simultaneous-update, current-output digital-to-analog converters (DACs) designed for superior performance in communications systems requiring analog signal reconstruction with low distortion and low-power operation. The MAX5189 provides equal specifications, with on-chip precision resistors for voltage output operation. The MAX5186/MAX5189 are designed for a 10pV-s glitch operation to minimize unwanted spurious signal components at the output. An on-board 1.2V bandgap circuit provides a well-regulated, low-noise reference that can be disabled for external reference operation.

The MAX5186/MAX5189 are designed to provide a high level of signal integrity for the least amount of power dissipation. Both DACs operate from a single supply voltage of 2.7V to 3.3V. Additionally, these DACs have three modes of operation: normal, low-power standby, and complete shutdown, which provides the lowest possible power dissipation with a 1 μ A (max) shutdown current. A fast wake-up time (0.5 μ s) from standby mode to full DAC operation allows power conservation by activating the DACs only when required.

The MAX5186/MAX5189 are packaged in a 28-pin QSOP and are specified for the extended (-40°C to +85°C) temperature range. For higher resolution, dual 10-bit versions, refer to the MAX5180/MAX5183 data sheet.

Applications

- Signal Reconstruction of I and Q Transmit Signals
- Digital Signal Processing
- Arbitrary Waveform Generation (AWG)
- Imaging Applications

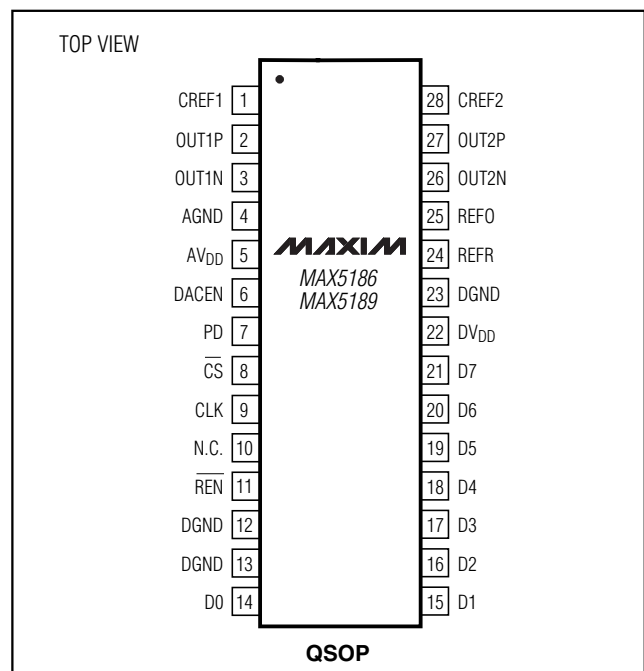
Features

- ◆ 2.7V to 3.3V Single-Supply Operation
- ◆ Wide Spurious-Free Dynamic Range: 70dB at $f_{OUT} = 2.2\text{MHz}$
- ◆ Fully Differential Outputs for Each DAC
- ◆ $\pm 0.5\%$ FSR Gain Mismatch at $f_{OUT} = 2.2\text{MHz}$
- ◆ $\pm 0.15^\circ$ Phase Mismatch at $f_{OUT} = 2.2\text{MHz}$
- ◆ Low-Current Standby or Full Shutdown Modes
- ◆ Internal 1.2V, Low-Noise Bandgap Reference
- ◆ Small 28-Pin QSOP Package

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5186BEEI	-40°C to +85°C	28 QSOP
MAX5189BEEI	-40°C to +85°C	28 QSOP

Pin Configuration



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ABSOLUTE MAXIMUM RATINGS

AVDD, DVDD to AGND, DGND	-0.3V to +6V	Continuous Power Dissipation (TA = +70°C)	
Digital Input to DGND.....	-0.3V to +6V	28-Pin QSOP (derate 10.8mW/°C above +70°C)	860.2mW
OUT1P, OUT1N, OUT2P, OUT2N, CREF1, CREF2 to AGND	-0.3V to +6V	Operating Temperature Ranges	
REF0, REFR to AGND.....	-0.3V to +6V	MAX518_BEE1.....	-40°C to +85°C
AGND to DGND.....	-0.3V to +0.3V	Storage Temperature Range	-65°C to +150°C
AVDD to DVDD.....	±3.3V	Lead Temperature (soldering, 10s)	+300°C
Maximum Current into Any Pin.....	50mA		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AVDD = DVDD = 3V, AGND = DGND = 0, fCLK = 40MHz, IFS = 1mA, 400Ω differential output, CL = 5pF, TA = TMIN to TMAX, unless otherwise noted. ≥ +25°C guaranteed by production test, < +25°C guaranteed by design and characterization. Typical values are at TA = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution	N		8			Bits
Integral Nonlinearity	INL		-1	±0.25	+1	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic	-1	±0.25	+1	LSB
Offset Error		MAX5186	-1		+1	LSB
		MAX5189	-4		+4	
Gain Error		(Note 1)	-20	±4	+20	LSB
DYNAMIC PERFORMANCE						
Output Settling Time		To ±0.5LSB error band		25		ns
Glitch Impulse				10		pV-s
Spurious-Free Dynamic Range to Nyquist	SFDR	fCLK = 40MHz	fOUT = 550kHz		72	dBc
			fOUT = 2.2MHz, TA = +25°C	57	70	
Total Harmonic Distortion to Nyquist	THD	fCLK = 40MHz	fOUT = 550kHz		-70	dBc
			fOUT = 2.2MHz, TA = +25°C		-68	
Signal-to-Noise-Ratio to Nyquist	SNR	fCLK = 40MHz	fOUT = 550kHz		52	dB
			fOUT = 2.2MHz, TA = +25°C	46	52	
DAC-to-DAC Output Isolation		fOUT = 2.2MHz		-60		dB
Clock and Data Feedthrough		All 0s to all 1s		50		pV-s
Output Noise				10		pA/√Hz
Gain Mismatch Between DAC Outputs		fOUT = 2.2MHz, TA = +25°C		±0.5	±1	% FSR
Phase Mismatch Between DAC Outputs		fOUT = 2.2MHz		±0.15		degrees

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ELECTRICAL CHARACTERISTICS (continued)

(AVDD = DVDD = 3V, AGND = DGND = 0, fCLK = 40MHz, IFS = 1mA, 400Ω differential output, CL = 5pF, TA = TMIN to TMAX, unless otherwise noted. ≥ +25°C guaranteed by production test, < +25°C guaranteed by design and characterization. Typical values are at TA = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG OUTPUT						
Differential Full-Scale Output Voltage	VFS			400		mV
Voltage Compliance Range			-0.3		0.8	V
Output Leakage Current		DACEN = 0, MAX5186 only	-1		1	μA
Full-Scale Output Current	IFS	MAX5186 only	0.5	1	1.5	mA
DAC External Output Resistor Load	RL	MAX5186 only		400		Ω
REFERENCE						
Output Voltage Range	VREFO		1.12	1.2	1.28	V
Output Voltage Temperature Drift	TCVREFO			50		ppm/°C
Reference Output Drive Capability	IREFO			10		μA
Reference Supply Rejection				0.5		mV/V
Current Gain (IFS / IREF)				8		mA/mA
POWER REQUIREMENTS						
Analog Power-Supply Voltage	AVDD		2.7		3.3	V
Analog Supply Current	I _{AVDD}	PD = 0, DACEN = 1, digital inputs at 0 or DVDD		2.7	5.0	mA
Digital Power-Supply Voltage	DVDD		2.7		3.3	V
Digital Supply Current	IDVDD	PD = 0, DACEN = 1, digital inputs at 0 or DVDD		4.2	5.0	mA
Standby Current	I _{STANDBY}	PD = 0, DACEN = 0, digital inputs at 0 or DVDD		1.0	1.5	mA
Shutdown Current	I _{SHDN}	PD = 1, DACEN = X, digital inputs at 0 or DVDD (X = don't care)		0.5	1	μA
LOGIC INPUTS AND OUTPUTS						
Digital Input Voltage High	V _{IH}		2			V
Digital Input Voltage Low	V _{IL}				0.8	V
Digital Input Current	I _{IN}	V _{IN} = 0 or DVDD			±1	μA
Digital Input Capacitance	C _{IN}			10		pF
TIMING CHARACTERISTICS						
DAC1 DATA to CLK Rise Setup Time	t _{DS1}			10		ns
DAC2 DATA to CLK Fall Setup Time	t _{DS2}			10		ns
DAC1 CLK Rise to DATA Hold Time	t _{DH1}			0		ns
DAC2 CLK Fall to DATA Hold Time	t _{DH2}			0		ns

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ELECTRICAL CHARACTERISTICS (continued)

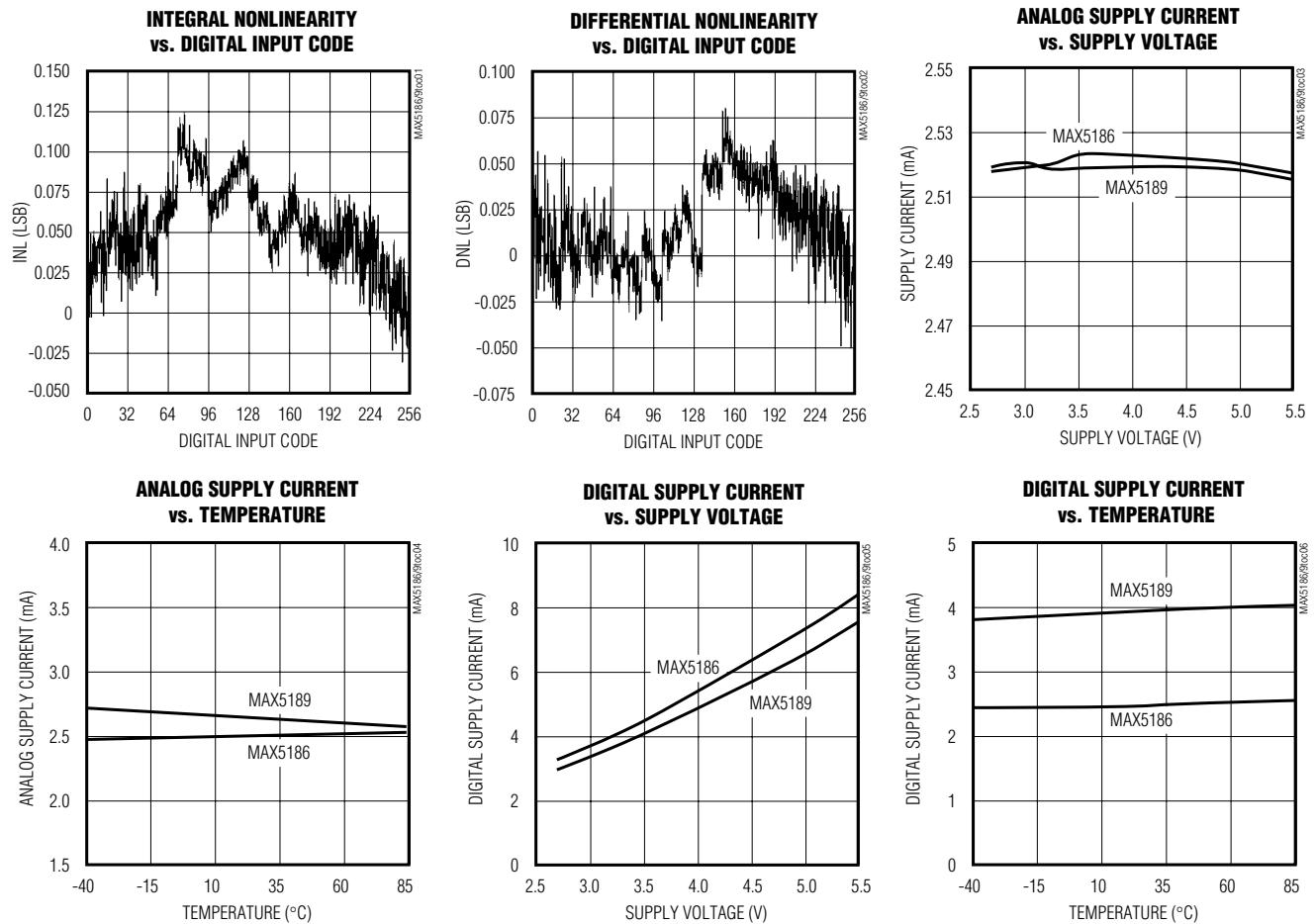
($V_{DD} = DV_{DD} = 3V$, $AGND = DGND = 0$, $f_{CLK} = 40MHz$, $I_{FS} = 1mA$, 400Ω differential output, $C_L = 5pF$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. $\geq +25^\circ C$ guaranteed by production test, $< +25^\circ C$ guaranteed by design and characterization. Typical values are at $T_A = +25^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
\overline{CS} Fall to CLK Rise Time				5		ns
\overline{CS} Fall to CLK Fall Time				5		ns
DACEN Rise Time to V_{OUT}				0.5		μs
PD Fall Time to V_{OUT}				50		μs
Clock Period	t_{CLK}		25			ns
Clock High Time	t_{CH}		10			ns
Clock Low Time	t_{CL}		10			ns

Note 1: Excludes reference and reference resistor (MAX5189) tolerance.

Typical Operating Characteristics

($V_{DD} = DV_{DD} = 3V$, $AGND = DGND = 0$, 400Ω differential output, $I_{FS} = 1mA$, $C_L = 5pF$, $T_A = +25^\circ C$, unless otherwise noted.)

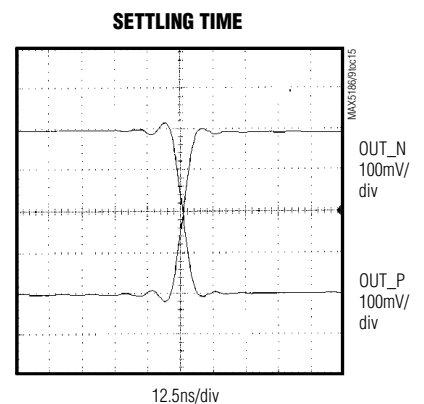
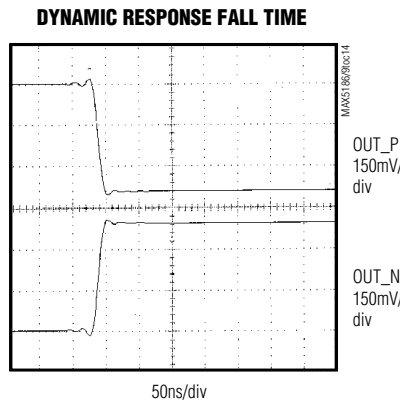
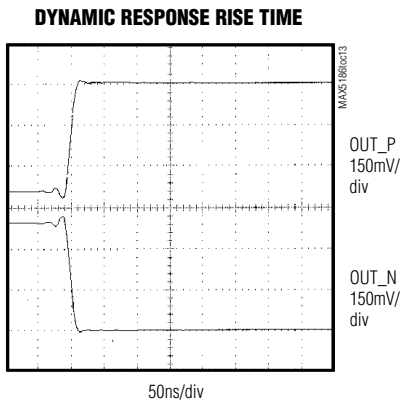
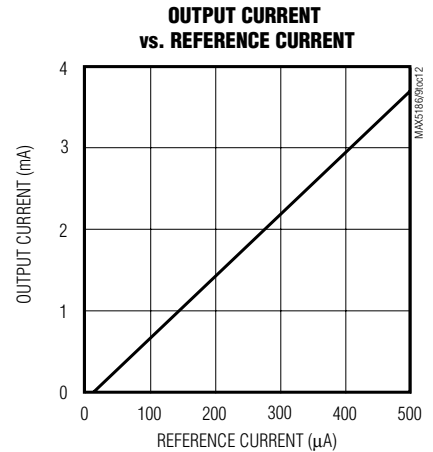
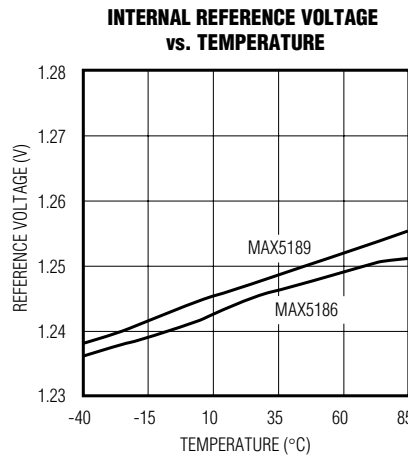
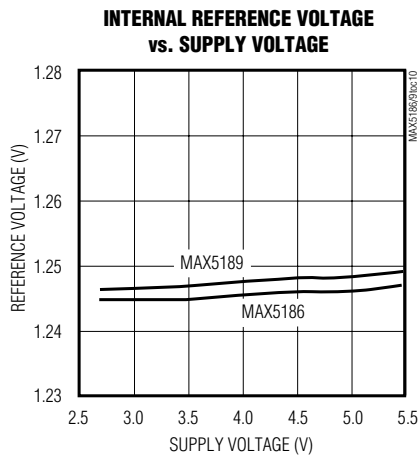
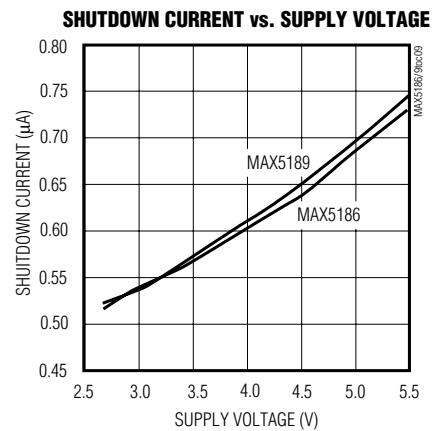
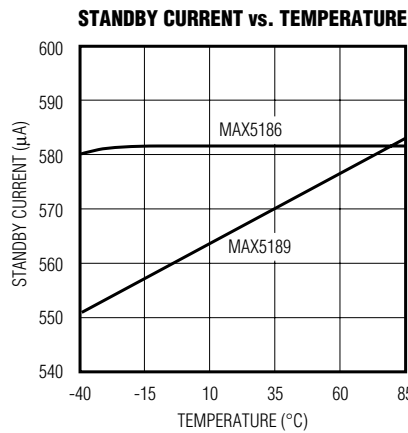
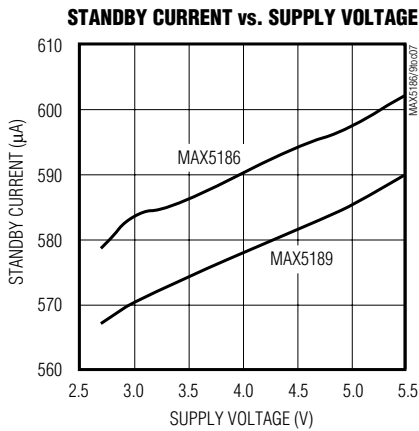


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Typical Operating Characteristics (continued)

($V_{DD} = DV_{DD} = 3V$, $AGND = DGND = 0$, 400Ω differential output, $I_{FS} = 1mA$, $C_L = 5pF$, $T_A = +25^\circ C$, unless otherwise noted.)

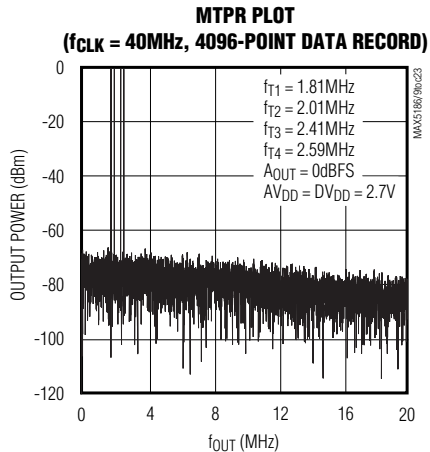
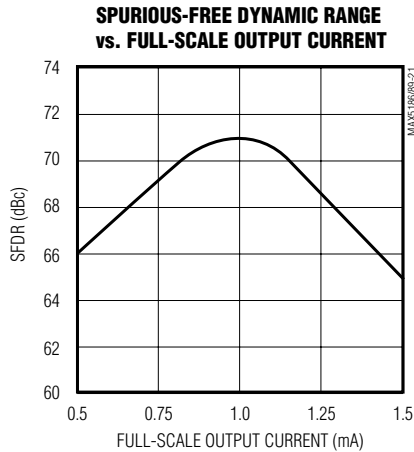
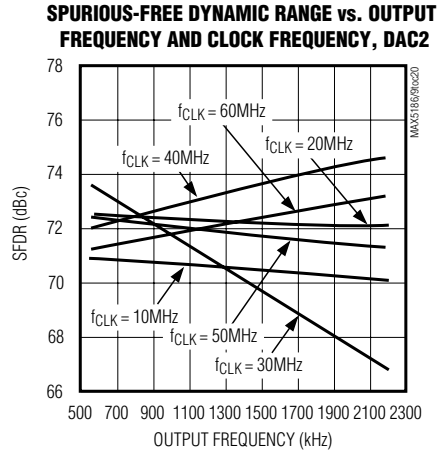
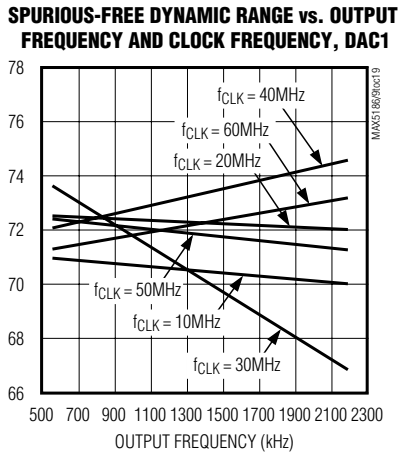
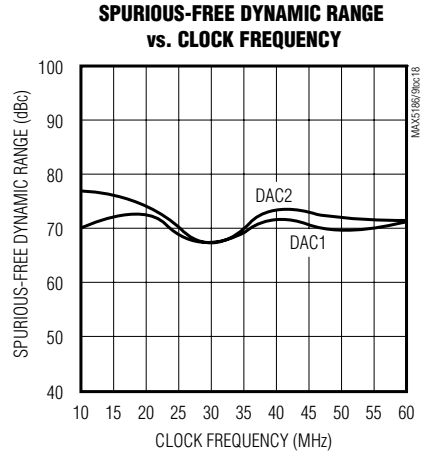
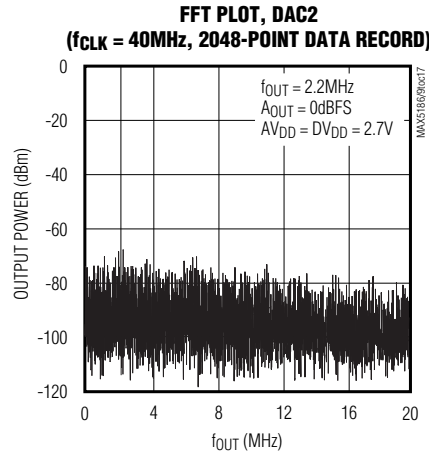
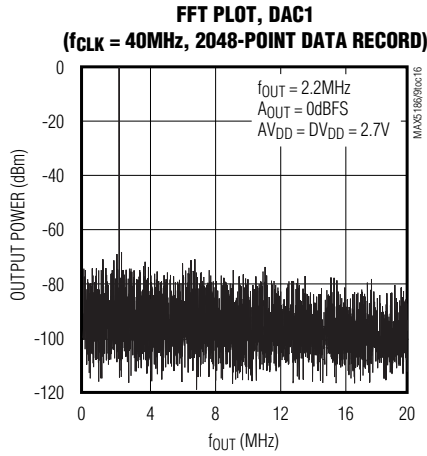
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Typical Operating Characteristics (continued)

($V_{DD} = DV_{DD} = 3V$, $AGND = DGND = 0$, 400Ω differential output, $I_{FS} = 1mA$, $C_L = 5pF$, $T_A = +25^\circ C$, unless otherwise noted.)



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Pin Description

MAX5186/MAX5189

PIN	NAME	FUNCTION
1	CREF1	Reference Bias Bypass, DAC1
2	OUT1P	Positive Analog Output, DAC1. Current output for MAX5186; voltage output for MAX5189.
3	OUT1N	Negative Analog Output, DAC1. Current output for MAX5186; voltage output for MAX5189.
4	AGND	Analog Ground
5	AVDD	Analog Positive Supply, 2.7V to 3.3V
6	DACEN	DAC Enable, Digital Input 0: Enter DAC standby mode with PD = DGND. 1: Power-up DAC with PD = DGND. X: Enter shutdown mode with PD = DVDD (X = don't care).
7	PD	Power-Down Select 0: Enter DAC standby mode (DACEN = DGND) or power-up DAC (DACEN = DVDD). 1: Enter shutdown mode.
8	$\overline{\text{CS}}$	Active-Low Chip Select
9	CLK	Clock input
10	N.C.	No Connect. Do not connect to this pin.
11	$\overline{\text{REN}}$	Active-Low Reference Enable. Connect to DGND to activate on-chip 1.2V reference.
12	DGND	Digital Ground
13	DGND	Digital Ground
14	D0	Data Bit D0 (LSB)
15–20	D1–D6	Data Bits D1–D6
21	D7	Data Bit D7 (MSB)
22	DVDD	Digital Supply, 2.7V to 3.3V
23	DGND	Digital Ground
24	REFR	Reference Input
25	REFO	Reference Output
26	OUT2N	Negative Analog Output, DAC2. Current output for MAX5186; voltage output for MAX5189.
27	OUT2P	Positive Analog Output, DAC2. Current output for MAX5186; voltage output for MAX5189.
28	CREF2	Reference Bias Bypass, DAC2

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Detailed Description

The MAX5186/MAX5189 are dual, 8-bit digital-to-analog converters (DACs) capable of operating with clock speeds up to 40MHz. Each of these dual converters consists of separate input and DAC registers, followed by a current source array capable of generating up to 1.5mA full-scale output current (Figure 1). An integrated 1.2V voltage reference and control amplifier determine the data converters' full-scale output currents/voltages. Careful reference design ensures close gain matching and excellent drift characteristics. The MAX5189's voltage output operation features matched 400Ω on-chip resistors that convert the current array current into a voltage.

Internal Reference and Control Amplifier

The MAX5186/MAX5189 provide an integrated 50ppm/°C, 1.2V, low-noise bandgap reference that can be disabled and overridden by an external reference voltage. REFO serves either as an external reference input or an integrated reference output. If $\overline{\text{REN}}$ is connected to DGND, the internal reference is selected and REFO provides a 1.2V output. Due to its limited 10μA output drive capability, REFO must be buffered with an external amplifier if heavier loading is required.

The MAX5186/MAX5189 also employ a control amplifier designed to simultaneously regulate the full-scale output current (IFS) for both outputs of the devices. The output current is calculated as follows:

$$\text{IFS} = 8 \times \text{IREF}$$

where IREF is the reference output current (IREF = VREFO/RSET) and IFS is the full-scale output current. RSET is the reference resistor that determines the amplifier's output current on the MAX5186 (Figure 2). This current is mirrored into the current source array where it is equally distributed between matched current segments and summed to valid output current readings for the DACs.

The MAX5189 converts each output current (DAC1 and DAC2) into an output voltage (VOUT1, VOUT2) with two internal, ground-referenced 400Ω load resistors. Using the internal 1.2V reference voltage, the MAX5189's integrated reference output-current resistor (RSET = 9.6kΩ) sets IREF to 125μA and IFS to 1mA.

External Reference

To disable the MAX5186/MAX5189's internal reference, connect $\overline{\text{REN}}$ to DVDD. A temperature-stable, external reference may now be applied to drive the REFO pin to set the full-scale output (Figure 3). Choose a reference capable of supplying at least 150μA to drive the bias circuit that generates the cascode current for the current array. For improved accuracy and drift performance, choose a fixed output voltage reference such as the 1.2V, 25ppm/°C MAX6520 bandgap reference.

Standby Mode

To enter the lower power standby mode, connect digital inputs PD and DACEN to DGND. In standby, both the reference and the control amplifier are active with the current array inactive. To exit this condition, DACEN must be pulled high with PD held at DGND. Both the MAX5186/MAX5189 typically require 50μs to wake up and let both outputs and reference settle.

Shutdown Mode

For lowest power consumption, the MAX5186/MAX5189 provide a power-down mode in which the reference, control amplifier, and current array are inactive and the DACs' supply current is reduced to 1μA. To enter this mode, connect PD to DVDD. To return to active mode, connect PD to DGND and DACEN to DVDD. About 50μs are required for the parts to leave shutdown mode and settle to their outputs' values prior to shutdown. Table 1 lists the power-down mode selection.

Timing Information

The MAX5186/MAX5189 dual DACs write to their outputs simultaneously (Figure 4). On the falling edge of the clock, the input data for DAC2 is preloaded into a latch. On the rising edge of the clock, input data for DAC1 is loaded to the DAC1 register, and the preloaded DAC2 data in the latch is loaded to the DAC2 register.

Outputs

The MAX5186 outputs are designed to supply full-scale output currents of 1mA into 400Ω loads in parallel with a capacitive load of 5pF. The MAX5189 features integrated 400Ω resistors that restore the array currents to proportional, differential voltages of 400mV. These differential output voltages can then be used to drive a balun transformer or a low-distortion, high-speed operational amplifier to convert the differential voltage into a single-ended voltage.

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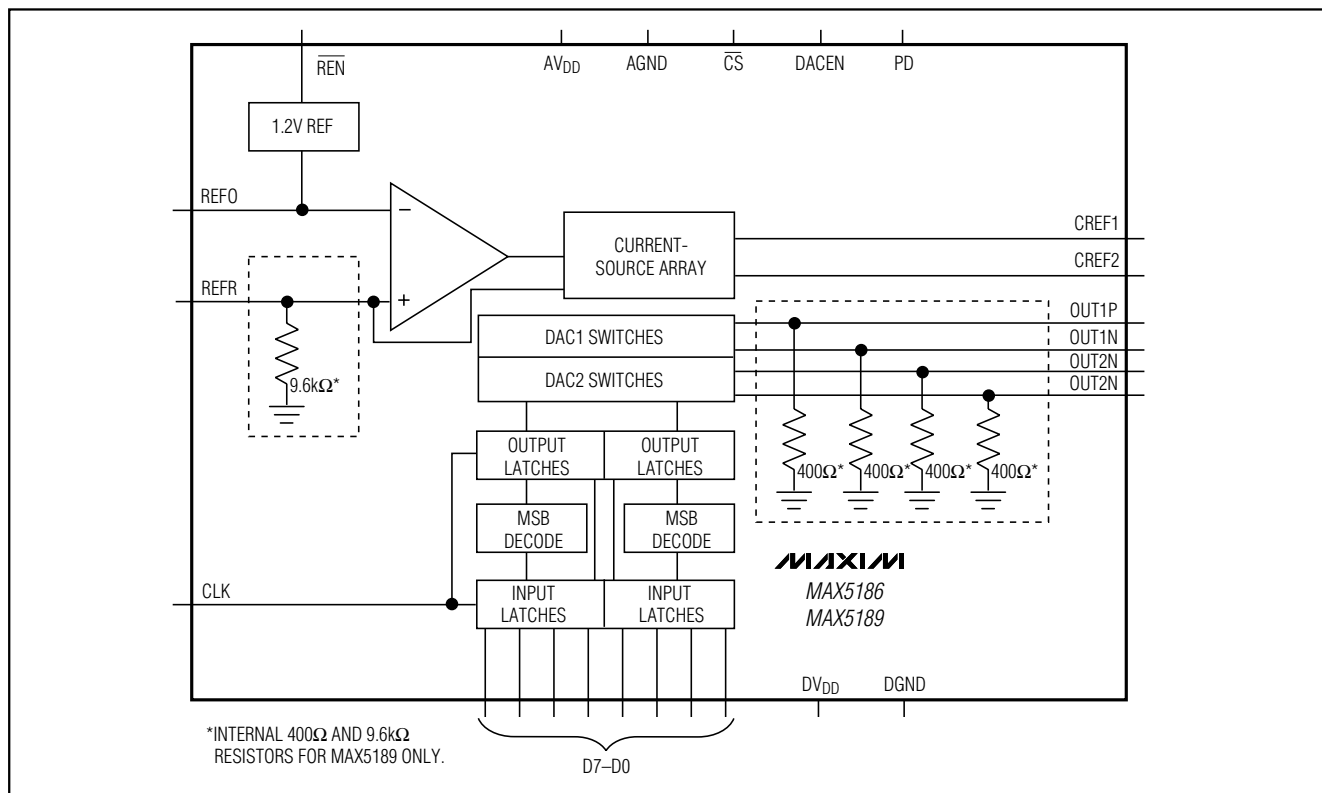


Figure 1. Functional Diagram

Applications Information

Static and Dynamic Performance Definitions

Integral Nonlinearity (INL)

Integral nonlinearity is the deviation of the values on an actual transfer function from either a best straight-line fit (closest approximation to the actual transfer curve) or a line drawn between the endpoints of the transfer function, once offset and gain errors have been nullified. The MAX5186/MAX5189 use a straight-line endpoint fit for INL (and DNL) and the deviations are measured at every individual step.

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between an actual step height and the ideal value of 1LSB. A DNL error specification no more negative than -1LSB guarantees a monotonic transfer function.

Offset Error

The offset error is the difference between the ideal and the actual offset current/voltage. For the MAX5186/MAX5189, the offset error is the midpoint value of the

transfer function determined by the endpoints of a straight-line endpoint fit. This error affects all codes by the same amount.

Gain Error

Gain error is the difference between the ideal and the actual output value range. This range represents the output when all digital inputs are set to 1 minus the output when all digital inputs are set to 0.

Glitch Impulse

A glitch is generated when a DAC switches between two codes. The largest glitch is usually generated around the midscale transition, when the input pattern transitions from 011...111 to 100...000. This occurs due to timing variations between the bits. The glitch impulse is found by integrating the voltage of the glitch at the midscale transition over time. The glitch impulse is usually specified in pV-s.

Settling Time

The settling time is the amount of time required from the start of a transition until the DAC output settles its new output value to within the converter's specified accuracy.

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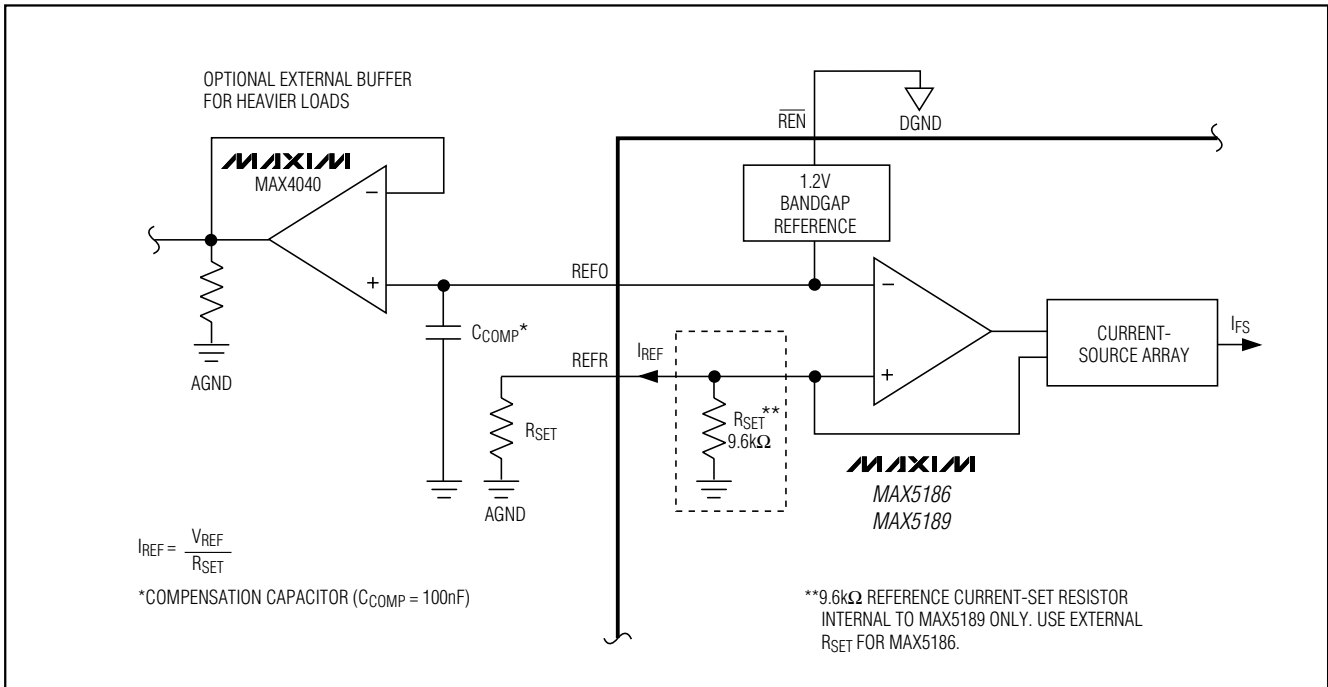


Figure 2. Setting I_{FS} with the Internal 1.2V Reference and the Control Amplifier

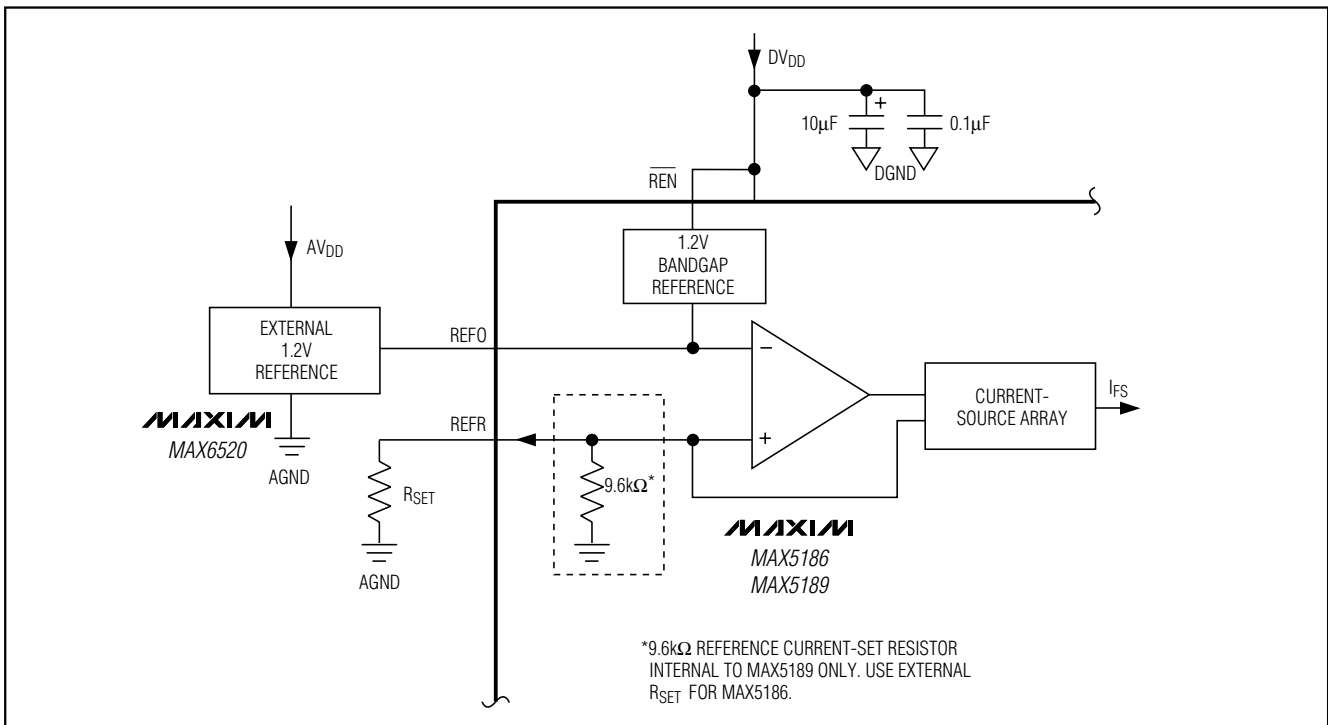


Figure 3. MAX5186/MAX5189 with External Reference

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Table 1. Power-Down Mode Selection

PD (POWER-DOWN SELECT)	DACEN (DAC ENABLE)	POWER-DOWN MODE	OUTPUT STATE	
0	0	Standby	MAX5186	High-Z
			MAX5189	AGND
0	1	Wake-Up	Last state prior to standby mode	
1	X	Shutdown	MAX5186	High-Z
			MAX5189	AGND

X = Don't care

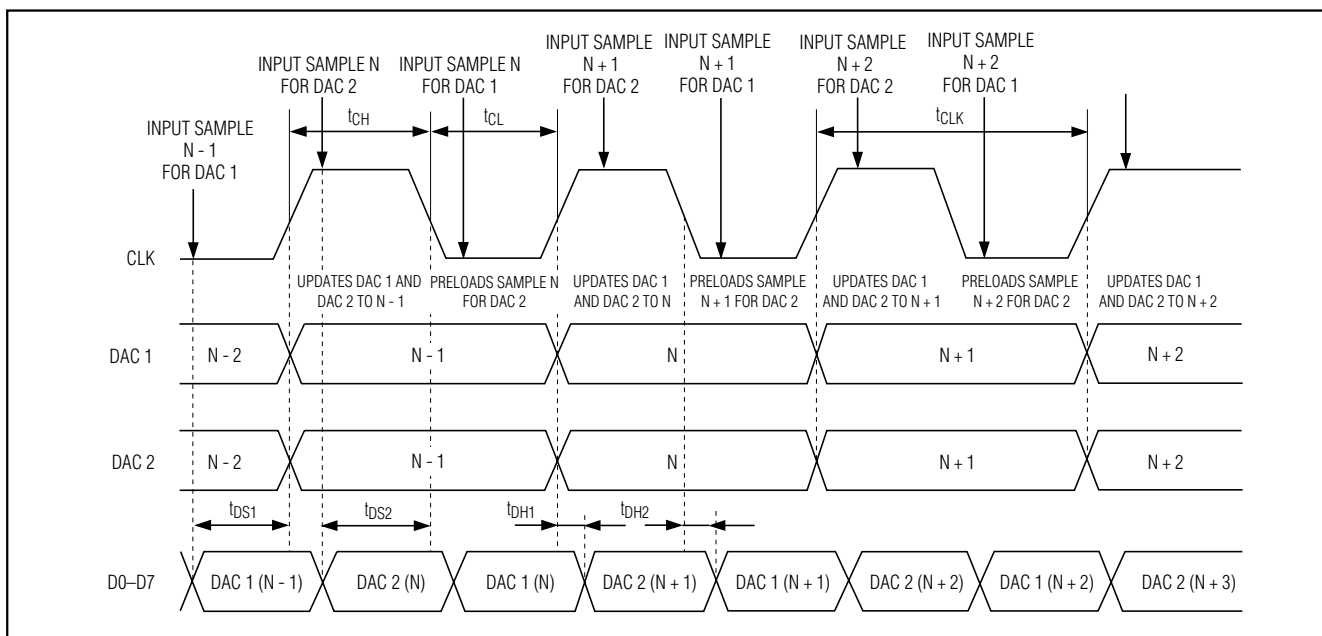


Figure 4. Timing Diagram

Digital Feedthrough

Digital feedthrough is the noise generated on a DAC's output when any digital input transitions. Proper board layout and grounding will significantly reduce this noise, but there will always be some feedthrough caused by the DAC itself.

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of the input signal's N harmonics to the fundamental itself. This is expressed as:

$$THD = 20 \times \log \left(\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \dots + V_N^2}}{V_1} \right)$$

where V_1 is the fundamental amplitude, and V_2 through V_N are the amplitudes of the 2nd- through Nth-order harmonics.

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio of RMS amplitude of the carrier frequency (maximum signal component) to the RMS value of the next largest noise or harmonic distortion component. SFDR is usually measured in dBc with respect to the carrier frequency amplitude or in dBFS with respect to the DAC's full-scale range. Depending on its test condition, SFDR is observed within a predefined window or to Nyquist. In the case of the MAX5186/MAX5189, the SFDR performance is measured for a 0dBFS output amplitude and analyzed within the Nyquist window.

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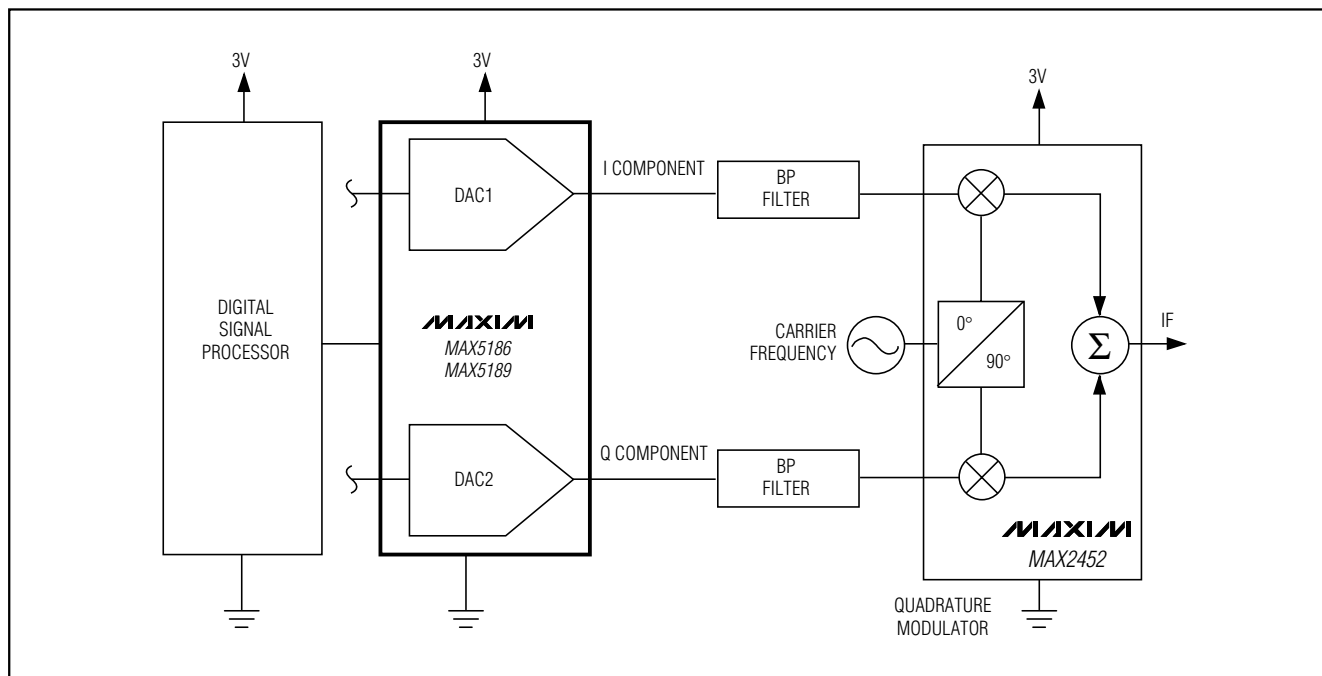


Figure 6. Using the MAX5186/MAX5189 for I/Q Signal Reconstruction

Grounding and Power-Supply Decoupling

Grounding and power-supply decoupling strongly influence the MAX5186/MAX5189's performance. Unwanted digital crosstalk may couple through the input, reference, power-supply, and ground connections, which may affect dynamic specifications like signal-to-noise ratio or SFDR. In addition, electromagnetic interference (EMI) can either couple into or be generated by the MAX5186/MAX5189. Therefore, grounding and power-supply decoupling guidelines for high-speed, high-frequency applications should be closely followed.

First, a multilayer printed circuit (PC) board with separate ground and power-supply planes is recommended. High-speed signals should be run on controlled impedance lines directly above the ground plane. Since the MAX5186/MAX5189 have separate analog and digital ground buses (AGND and DGND, respectively), the PC board should also have separate analog and digital ground sections with only one point connecting the two. Digital signals should run above the digital ground plane, and analog signals should run above the analog ground plane. Digital signals should be kept far away from the sensitive analog reference and clock input.

Both devices have two power-supply inputs: analog V_{DD} (AV_{DD}) and digital V_{DD} (DV_{DD}). Each AV_{DD} input should be decoupled with parallel $10\mu\text{F}$ and $0.1\mu\text{F}$ ceramic-chip capacitors. These capacitors should be as close to the pin as possible, and their opposite ends should be as close to the ground plane as possible. The DV_{DD} pins should also have separate $10\mu\text{F}$ and $0.1\mu\text{F}$ capacitors adjacent to their respective pins. Try to minimize analog load capacitance for proper operation. For best performance, it is recommended to bypass CREF1 and CREF2 with low-ESR $0.1\mu\text{F}$ capacitors to AV_{DD} .

The power-supply voltages should also be decoupled with large tantalum or electrolytic capacitors at the point they enter the PC board. Ferrite beads with additional decoupling capacitors forming a pi network can also improve performance.

Chip Information

TRANSISTOR COUNT: 9464
SUBSTRATE CONNECTED TO AGND

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Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°

DIM	INCHES		MILLIMETERS		N
	MIN.	MAX.	MIN.	MAX.	
D	.189	.196	4.80	4.98	16 AA
S	.0020	.0070	0.05	0.18	
X	.107	.123	2.72	3.12	
D	.337	.344	8.56	8.74	20 AB
S	.0500	.0550	1.270	1.397	
D	.337	.344	8.56	8.74	24 AC
S	.0250	.0300	0.635	0.762	
D	.386	.393	9.80	9.98	28 AD
S	.0250	.0300	0.635	0.762	
X	.271	.287	6.88	7.29	

NOTES:

- D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
- MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
- HEAT SLUG DIMENSIONS X AND Y APPLY ONLY TO 16 AND 28 LEAD POWER-QSOP PACKAGES.
- CONTROLLING DIMENSIONS: INCHES.
- MEETS JEDEC MO137.

VARIATIONS:

MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, QSOP, 150°, .025° LEAD PITCH
APPROVAL: DOCUMENT CONTROL NO. 21-0055 REV C 1/1

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14 Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600